

DATA SHEET

SKY65040-360LF: Low Noise Amplifier 1.5–2.4 GHz

Applications

- Wireless infrastructure including GSM, CDMA, W-CDMA, and TD-SCDMA
- Ultra low noise applications

Features

- Ultra low noise figure: 0.65 dB @ 1.95 GHz
- Excellent input and output return loss
- Adjustable gain: 15–25 dB @ 1.95 GHz
- High output 3rd order intercept: 34.5 dBm @ 65 mA
- Output P₁ dB: 16 dBm @ 1.95 GHz
- Single, positive DC supply voltage
- Adjustable supply current, 30–100 mA
- Low cost small 8-lead QFN 2 x 2 mm package
- Available lead (Pb)-free, RoHS-compliant, and Green™, MSL-1 @ 260 °C per JEDEC J-STD-020

Description

The SKY65040-360LF is a high performance, two-stage ultralow noise amplifier fabricated from Skyworks advanced pHEMT process and packaged in a QFN 8L 2 x 2 mm package. The device features excellent input and output return loss and an integrated interstage matching network. The amplifier's ultralow noise figure, high gain and excellent third order intercept (IP3) allows it to be used in various receiver and transmitter applications.

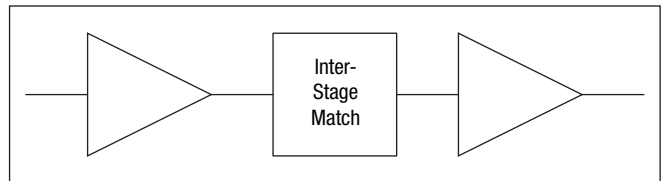
The SKY65040-360LF is lead (Pb)-free and RoHS-compliant.

NEW

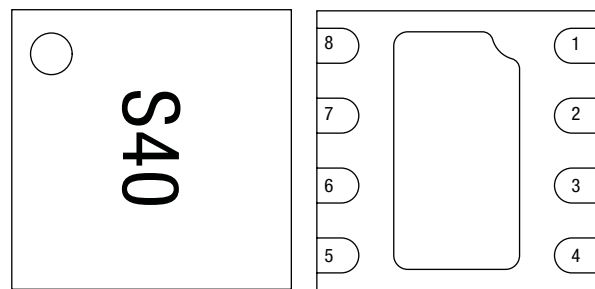


Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.

Functional Block Diagram



8-Lead QFN 2 x 2 mm Package



TOP VIEW

BOTTOM VIEW

Pin Configuration

Pin 1: V _{DD1}	Pin 5: Feedback
Pin 2: RFIN	Pin 6: No Connection
Pin 3: BIAS1	Pin 7: RFOUT/V _{DD2}
Pin 4: BIAS2	Pin 8: No Connection

Operating Characteristics

T = 25 °C, Z₀ = 50 Ω, V_{DD} = 5 V, I_{DD} = 65 mA, parameters include recommended 1950 MHz matching network unless otherwise noted

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Noise figure ⁽¹⁾	NF			0.65	1	dB
Small signal gain	S ₂₁		23.5	25	26.5	dB
Input return loss	S ₁₁			-25		dB
Output return loss	S ₂₂			-15		dB
Reverse isolation	S ₁₂			-34		dB
Output third order intercept point	OIP3	5 MHz spacing, P _{IN} = -18 dBm per tone		34.5		dBm
1 dB output compression point	OP ₁ dB			16		dBm
Stability		Unconditionally stable up to 18 GHz				

1. Loss of input RF connector and board trace de-embedded from measurement

Absolute Maximum Ratings

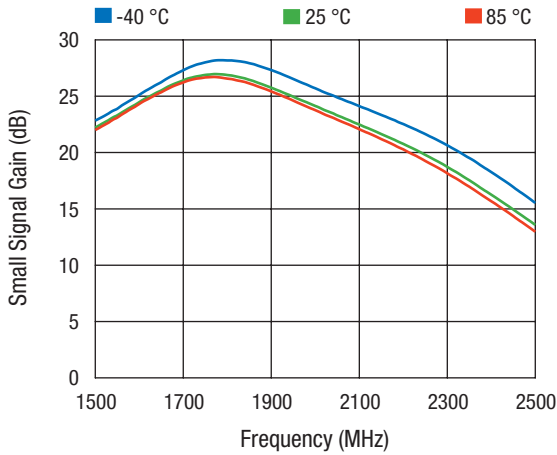
Characteristic	Value
Supply voltage (V _{DD})	5.5 V
RF input power (P _{IN})	10 dBm
Supply current stage one (I _{DS1})	50 mA
Supply current stage two (I _{DS2})	100 mA
Power dissipation (P _{DISS})	240 mW
Junction temperature (T _J)	150 °C
Storage temperature range (T _{ST})	-65 °C to +125 °C
Operating temperature range (T _{OP})	-40 °C to +85 °C
Thermal resistance (Θ _{JC})	47 °C/W

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

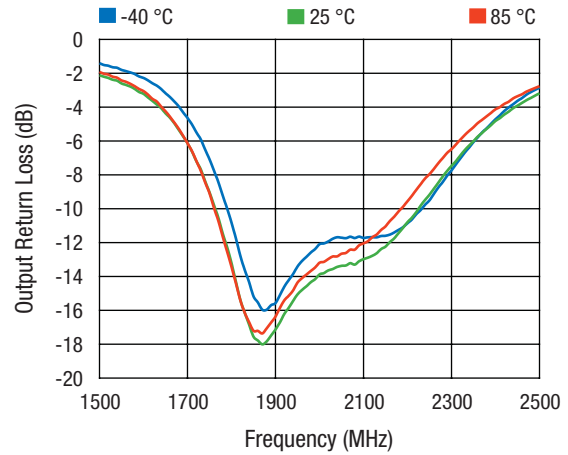
CAUTION: *Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.*

Typical Performance Data

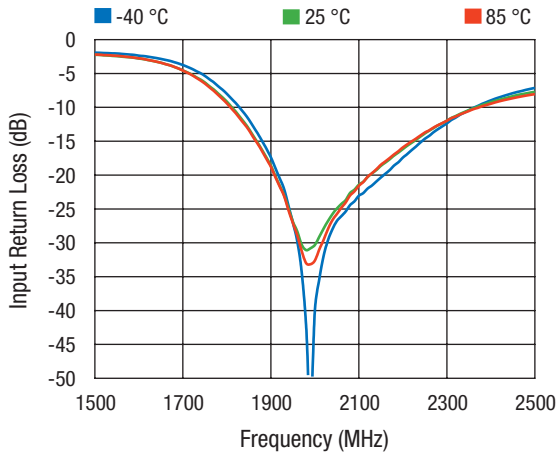
T = 25 °C, Z₀ = 50 Ω, V_{DD} = 5 V, I_{DD} = 65 mA, parameters include recommended 1950 MHz matching network unless otherwise noted



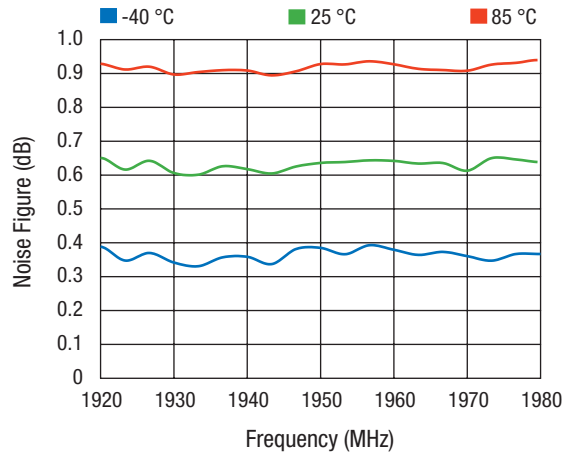
Small Signal Gain vs. Frequency for Multiple Temperatures, P_{IN} = -20 dBm



Output Return Loss vs. Frequency for Multiple Temperatures, P_{IN} = -20 dBm



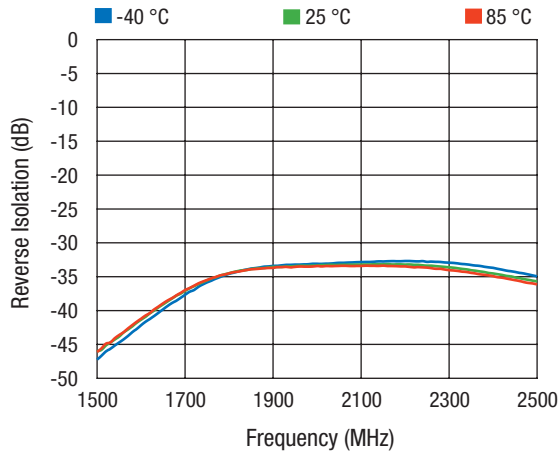
Input Return Loss vs. Frequency for Multiple Temperatures, P_{IN} = -20 dBm



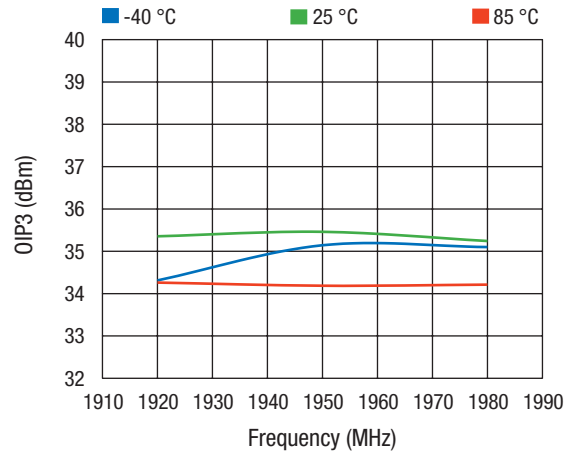
Noise Figure vs. Frequency for Multiple Temperatures, Input RF Connector and Board Trace De-embedded from Measurement

Typical Performance Data

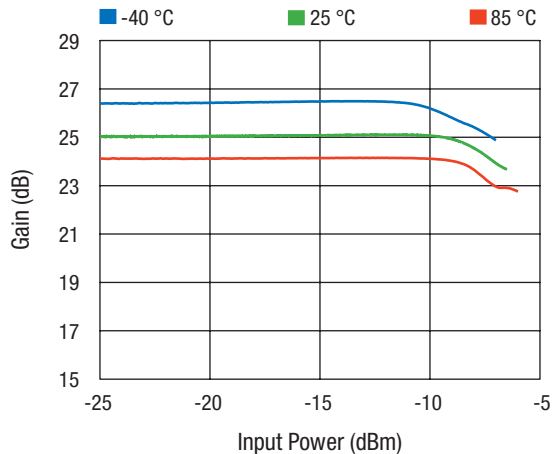
T = 25 °C, Z₀ = 50 Ω, V_{DD} = 5 V, I_{DD} = 65 mA, parameters include recommended 1950 MHz matching network unless otherwise noted



Reverse Isolation vs. Frequency for Multiple Temperatures, P_{IN} = -20 dBm



OIP3 vs. Frequency for Multiple Temperatures, P_{IN} = -18 dBm/Tone, 5 MHz Tone Spacing



Gain vs. Input Power for Multiple Temperatures, F = 1950 MHz

Theory of Operation

The SKY65040-360LF is a two stage low noise amplifier with an integrated interstage matching network. It is fabricated on Skyworks advanced pHEMT process and packaged in a QFN 8L 2 x 2 mm package. Using the recommended basic connections shown in the Evaluation Board Schematic, the device has a tested low noise figure of 0.65 dB and gain of 25 dB. The device allows designers to adjust current and gain without degrading noise figure.

The external matching network largely dictates the RF performance of the device. The matching network is required for operation and special care should be taken when designing a circuit board layout for the SKY65040-360LF. There are four separate sections to the external components; the input, output, biasing, and feedback components.

Biasing

To properly bias a depletion mode pHEMT, both the gate and drain of the device must be biased properly. At $V_{GS} = 0\text{ V}$ and $V_{DS} > 2\text{ V}$, the stage of the amplifier is in its saturated state and will draw the maximum amount of current, I_{DSS} . A V_{DS} of 5 V is recommended to ensure proper performance.

To eliminate the need of a negative DC supply, self-biasing should be used where a resistor is placed between one of the source leads and ground. A bypass capacitor should be placed in parallel to provide a RF ground and to ensure performance at the operating frequency remains unchanged. Current flows from drain to source through the resistor, resulting in the source voltage to be biased above DC ground. The gate pin of the device should be left unbiased at 0 V, thus creating the desired negative V_{GS} value. This largely simplifies the design by eliminating the need for a second DC supply. Resistor values for R1 and R2 can be changed to easily increase or decrease the bias current to a desired level.

The first stage is biased at 20% of I_{DSS} to achieve the best noise figure performance. The gain and current of the 2nd stage amplifier can be adjusted without degrading the overall noise figure. More current in the 2nd stage will yield better IP3 performance.

Components L3 and L5 are the RF bias choke inductors. These are required to block RF power and pass V_{DD} to the drain of each amplifier stage. Components C4 through C10 are bypass capacitors. R4 and R5 reduce the voltage presented at the drain of each stage of the device. The resistor values are optimized for OIP3 and P_1 dB performance.

Source Inductance

The effect of source inductance will vary with frequency. Too little source inductance will increase gain and high frequency stability, but at the cost of more in-band instability. Too much source inductance will decrease high frequency stability and gain, but improve in-band instability. It is very important to find the optimum tuning of source inductance that will balance all variables.

The trace present on the first stage amplifier (pin 3) is about 100 mils in length and about 6 mils wide. The electrical length of the line is 9.8 degrees at 1.95 GHz. When designing a board for the SKY65040-360LF, these exact dimensions should be used. The board trace length at pin 4 should be minimized.

Input and Output RF Matching Network

The input band pass matching network consists of five components. C1 serves as the input DC blocking capacitor. C2 and C3 provide high frequency stability and improved input return loss. L1 and L2 are responsible for the best noise match looking into the gate of the first stage amplifier. Excess board trace should be eliminated at the input of the device to minimize board losses. High Q components should be used to achieve the best noise figure of the amplifier. Murata GJM series capacitors and Coilcraft HP or CS series inductors are recommended. Any excess board or component loss on the input of the device will directly add to the total measured noise figure.

The output matching network is band pass network optimized for best output return loss.

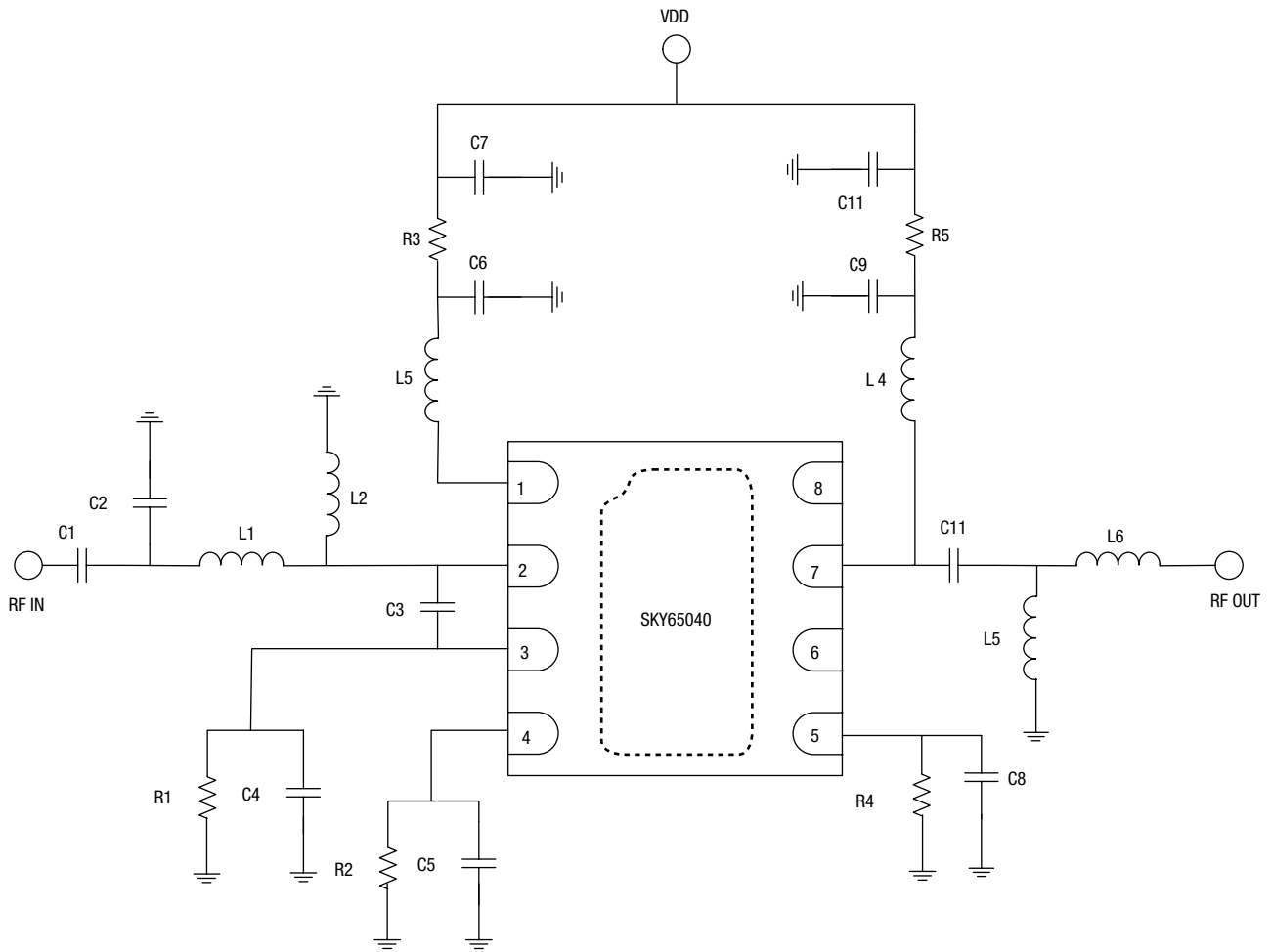
Feedback

Using feedback on the SKY65040-360LF is not necessary, but can be used to reduce gain without affecting other parameters. The default circuit configuration has 25 dB of gain, but can be reduced to about 18 dB. A recommended circuit that incorporates feedback is available upon request.

Measuring Noise Figure

Special care should be taken when making $< 1\text{ dB}$ noise figure measurements. Ideally, measurements should be made in an RF shield room. An Agilent MXA N9020A spectrum analyzer with an internal preamp paired with a N4001A smart noise source was used for all noise measurements. The smart noise source has an internal thermocouple which automatically sets the T_{COLD} setting on the analyzer. If a smart noise source is unavailable, a standard low ENR noise source should be used. Use an external thermocouple to manually adjust the T_{COLD} setting to ensure accurate results.

Evaluation Board Schematic



Layout and PCB Considerations

Please refer to the Recommended Board Layout. Input and output trace lengths have been minimized to reduce losses. All surface mount components are 0402 sized to reduce component parasitics. Use of 0603 or larger components is not recommended. Component spacing has also been minimized. The board is provisioned with two RF connectors and a DC launch. RF connector and board loss up to component C1 is approximately 0.1 dB at 1.95 GHz.

It is very important to place multiple ground vias as close to shunt components as possible. This will ensure proper grounding and circuit performance.

Board material is 10 mil VT47 FR4 with 1 oz. copper cladding. RF traces are 50 Ω with a 17.5 mil trace width and a 10 mil gap to ground.

Evaluation Board Test Procedure

Step 1: Connect RF test equipment to amplifier input/output SMA connectors

Step 2: Connect DC ground.

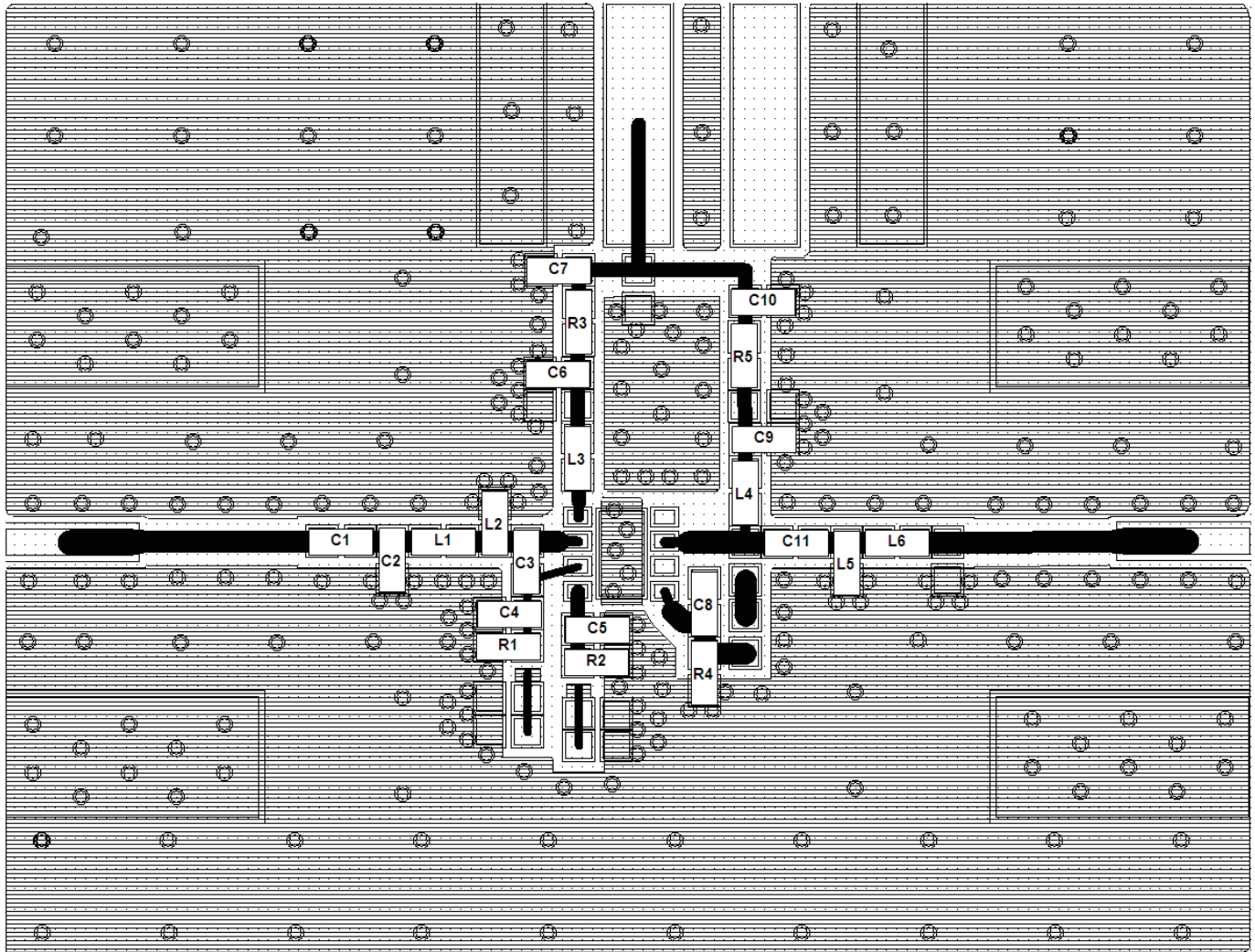
Step 3: Connect V_{DD} to a 5 V supply with a current limit of 100 mA. Verify that the board draws approximately 65 mA.

Step 4: Apply RF signal or noise source.

Recommended Evaluation Board Components for 1920–1980 MHz Operation

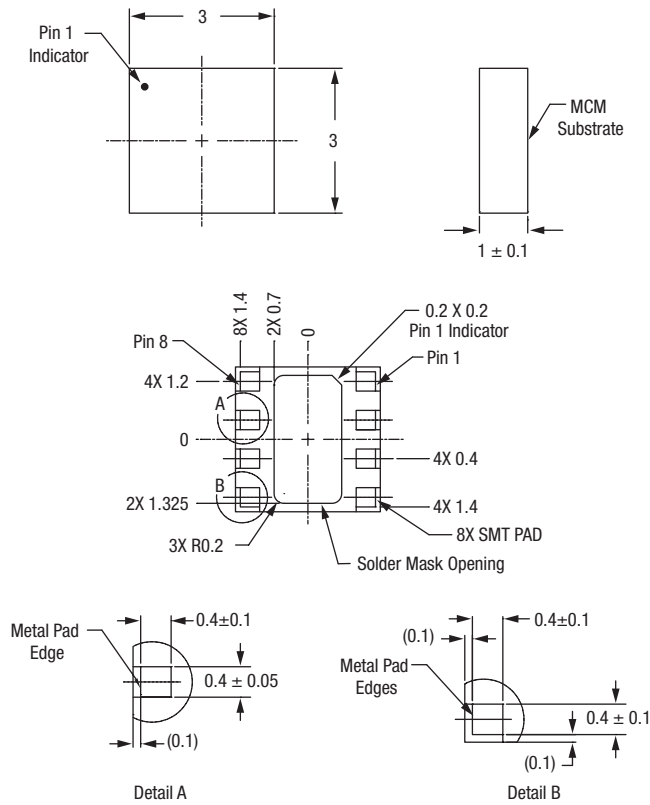
Component	Value	Size	Manufacturer	Description
C1	20pF	0402	Murata	GJM Series
C2	0.5 pF	0402	Murata	GJM Series
C3	0.2 pF	0402	Murata	GJM Series
C4	4700 pF	0402	Murata	GRM Series
C5	4700 pF	0402	Murata	GRM Series
C6	82 pF	0402	Murata	GRM Series
C7	4700 pF	0402	Murata	GRM Series
C8	0.3 pF	0402	Murata	GJM Series
C9	4700 pF	0402	Murata	GRM Series
C10	0.3 pF	0402	Murata	GJM Series
C11	8.2 pF	0402	Murata	GRM Series
L1	3.6 nH	0402	Coilcraft	HP Series
L2	11 nH	0402	Coilcraft	HP Series
L3	10 nH	0402	TDK	MLG Series
L4	7.5 nH	0402	TDK	MLG Series
L5	6.8 nH	0402	TDK	MLG Series
L6	3.9 nH	0402	TDK	MLG Series
R1	22 Ω	0402	Panasonic	
R2	9.1 Ω	0402	Panasonic	
R3	120 Ω	0402	Panasonic	
R4	3K Ω	0402	Panasonic	
R5	20 Ω	0402	Panasonic	

Recommended Board Layout

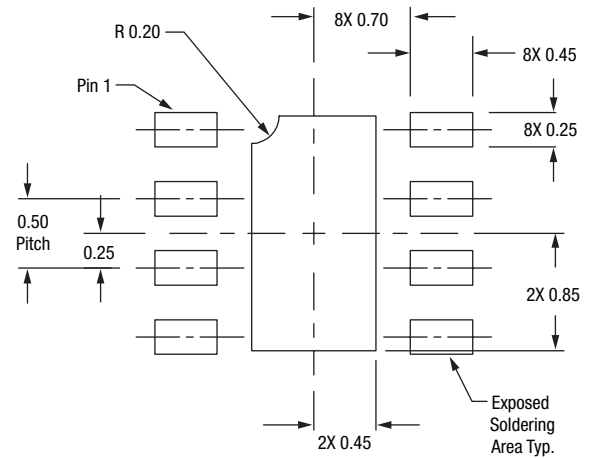


C1, C2, L1, and L2 are the input matching network.
 C11, L5, and L6 are the output matching network.
 R1, R3, and C4 are the bias components for the 1st stage amplifier.
 R2, R5, and C5 are the bias components for the 2nd stage amplifier.
 C6, C7, C9, and C10 are RF bypass capacitors.
 L3 and L4 are RF choke inductors.
 R4 and C8 provide DC grounding and high frequency stability when feedback is not used.

8-Lead 2 x 2 mm QFN Package Dimensions



Recommended Land Pattern



1. Dimensioning and tolerancing in accordance with asme y14.5m-1994 unless otherwise specified.
2. Dimensions are in millimeters unless otherwise specified.

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